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**Seventh Semester B.E. Degree Examination, December 2010**  
**DSP Algorithms and Architecture**

Time: 3 hrs.

Max. Marks:100

**Note: Answer any FIVE full questions, selecting  
at least TWO questions from each part.**

**PART – A**

- 1
  - a. An analog signal is sampled at the rate of 8 kHz. If 512 samples of this signal are used to compute DFT,  $X(k)$ , determine the analog and digital frequency spacing between adjacent  $X(k)$  elements. Also, determine analog and digital frequencies corresponding to  $k = 64$ . (06 Marks)
  - b. With a neat block diagram, explain the scheme of a DSP system. (08 Marks)
  - c. Let  $x(n) = [3, 2, -2, 0, 7]$ . It is interpolated using an interpolation filter  $b_k = [0.5, 1, 0.5]$ , with interpolation factor 2. Determine the interpolated sequence. (06 Marks)
  
- 2
  - a. Draw the schematic diagram of the saturation logic and explain the same. (06 Marks)
  - b. Explain how the circular addressing mode and bit reversal addressing mode are implemented in a digital signal processor. (08 Marks)
  - c. Explain the purpose of program sequencer. (06 Marks)
  
- 3
  - a. Identify the addressing mode of the source operand in each of the following instructions:
 

i) ADD *AR2, A	ii) ADD *AR2+, A	iii) ADD *AR2+%, A
iv) ADD #OFFh, A	v) ADD ABCDh, A	vi) ADD *AR2+OB, A

 (06 Marks)
  - b. Explain the PMST register. (08 Marks)
  - c. With an example each, explain immediate addressing mode, absolute addressing mode, direct addressing mode. (06 Marks)
  
- 4
  - a. Differentiate between MAC & MACD instructions by way of explaining them. (06 Marks)
  - b. Write a program to find the sum of series of signed numbers as specified below.
 
$$A = \sum_{i=410h}^{41Fh} x(i)$$
 Assume AR1 as pointer to  $x(i)$  and AR2 as counter for the numbers. (06 Marks)
  - c. By means of a figure, show the pipeline operation of the following sequences of TMS320C54XX instructions. Assume initial value of AR3 is 80h and the values stored in memory locations 80h, 81h, 82h as 1, 2 & 3.
 

```
LD *AR3+, A
ADD #1000h, A
STL A, *AR3+
```

 (08 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.  
2. Any revealing of identification, seal to evaluator and/or equations written eg,  $42+8 = 50$ , be treated as malpractice.

**PART – B**

- 5 a. i) Determine the value of each of the following 16-bit numbers represented using the given Q-notation 4400h as a Q0 number, 4400h as a Q15 number and 4400h as a Q7 number.
- ii) Represent each of the following as 16-bit numbers in the desired Q-notation. 0.3125 as a Q15 number, -0.3125 as a Q15 number and 3.125 as a Q7 number.

(06 Marks)

- b. Analyze the following program to answer the questions at the end. Assume that all specified data locations are on the same page starting at ao. Q15 notation is assumed.

```
.data
    ao    .word 6000h
    b1    .word 2000h
    xn    .word 4000h
    yn    .word 0h
    ynm1  .word 3000h

.text
    ld    #ao, dp
    ld    ao, t
    mpy  xn, a
    ld    b1, t
    mac  ynm1, a
    sth  a, 1, yn
```

- i) Determine the decimal values represented by yn.
- ii) Determine the equation for yn implemented by the above program. (06 Marks)

- c. Write a program to multiply two Q15 numbers. (08 Marks)

- 6 a. i) Derive the equation to implement a butterfly structure in DITFFT algorithm.
- ii) How many add/subtract and multiply operations are needed to compute the butterfly structure?
- iii) Determine the optimum scaling factor. (08 Marks)

- b. i) What minimum size FFT must be used to compute a DFT of 40 samples?
- ii) How many stages are required for FFT computation?
- iii) How many butterflies are there per stage?
- iv) How many butterflies are needed for the entire computation? (04 Marks)

- c. Write the subroutine for bit reverse address generation. Explain the same. (08 Marks)

- 7 a. Draw the timing diagram for memory interface for read-read-write sequence of operation. Explain the purpose of each signal involved. (08 Marks)

- b. Explain the register subaddressing technique for configuring DMA operation. (06 Marks)

- c. Explain the ADC interface in programmed I/O mode. (06 Marks)

- 8 a. With a neat block diagram and timing diagram for both transmit and receive, explain the signals involved in synchronous serial interface. (08 Marks)

- b. Explain how PPM signal is decoded at the receiving end using digital signal processor. (06 Marks)

- c. Write a pseudo algorithm for determining heart rate (HR), using the digital signal processor. (06 Marks)

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